IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	Confirmation No.: 2535
Yoshihiro TAKEMAE	Group Art Unit: 2185
Application No.: 10/687,591	Examiner: Daniel Y. KIM
Filed: October 20, 2003	Attorney Docket No.: 108397-00109
For: MEMORY SYSTEM	

REQUEST FOR ACKNOWLEDGEMENT OF PRIORITY DOCUMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 13, 2006

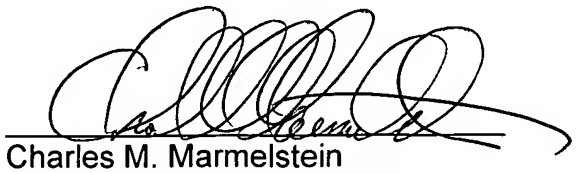
Sir:

In the Notice of Allowability dated October 26, 2006, the Examiner indicated that the certified copy of the priority document has not been received in the U.S. Patent and Trademark Office. The priority document was filed in parent Application Number 10/057,989, now U.S. Patent Number 6,650,593 B2, on January 29, 2002. Acknowledgement of the claim for priority was made on February 4, 2003, Paper Number 4.

The undersigned respectfully requests that the U.S. Patent and Trademark Office acknowledge receipt of the priority document for the above-identified application. Copies of the transmittal letter, the front cover of the priority document and the stamped postcard receipt are enclosed in support of this request.

Please charge any fee deficiency or credit any overpayment with respect to this paper to Counsel's Deposit Account Number 01-2300, referencing Docket Number 108397-00109.

Respectfully submitted,



Charles M. Marmelstein
Registration Number 25,895

Customer Number 004372
ARENT FOX PLLC
1050 Connecticut Avenue, NW, Suite 400
Washington, DC 20036-5339
Telephone: 202-857-6000
Fax: 202-638-4810

CMM/SCO:vmh

Enclosures: Transmittal Letter (copy)
Priority Document (copy of front cover)
Stamped Postcard Receipt (copy)

NONPROVISIONAL PATENT APPLICATION TRANSMITTAL RULE §1.53(b) IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Customer No. 004372
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
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Docket No. 108397-00063

Date: January 29, 2002

Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is a nonprovisional patent application:

For (Title): MEMORY SYSTEM

By (Inventors): Yoshihiro TAKEMAE

- ☒ 40 pages of Specification/Claims 1-15/Abstract are attached.
- ☒ Formal drawings (Figs. 1-17; 17 sheets are attached.
- ☒ A Declaration and Power of Attorney is attached.
- ☒ An assignment of the invention to FUJITSU LIMITED is attached, along with Form PTO-1595 and a check for $40.00.
- ☒ An Information Disclosure Statement is attached, along with Form PTO-1449, and 1 references.
- ☐ This application is entitled to Small Entity Status.
- ☐ A Preliminary Amendment is attached.
- ☐ Please amend the specification by inserting before the first line the sentence --This nonprovisional application claims the benefit of U.S. Provisional Application No. _____, filed _____. - -
- ☒ Priority of foreign application No. 2001-052484 filed February 27, 2001 in Japan is claimed under 35 U.S.C. §119.
- ☒ A certified copy of the above corresponding foreign application is attached.

The filing fee is calculated below and includes claim status after entry of any Preliminary Amendment noted above:

			SMALL ENTITY			LARGE ENTITY	
FOR:	NO. FILED	NO. EXTRA	RATE	FEE	OR	RATE	FEE
BASIC FEE				$ 370	OR		$ 740
TOTAL CLAIMS	15 - 20	= 0	x 9 =	$	OR	x 18	$
INDEP CLAIMS	1 - 3	= 0	x 42 =	$	OR	x 84	$
☐ MULTIPLE DEPENDENT CLAIMS			+140 =	$	OR	+280	$
			TOTAL	$	OR	TOTAL	$ 740

☒ A check in the amount of $780.00 ($740.00 for the filing fee and $40.00 for the Assignment Recordation Fee) is attached. Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300.

Respectfully submitted,

SIGNATURE ON ORIGINAL

Charles M. Marmelstein
Registration No. 25,895

CMM/ars

TECH/94284.1

日　本　国　特　許　庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office

出願年月日
Date of Application: ２００１年　２月２７日

出願番号
Application Number: 特願２００１－０５２４８４

出願人
Applicant(s): 富士通株式会社

２００１年１１月　２日

特許庁長官
Commissioner,
Japan Patent Office

及川耕造

出証番号　出証特２００１－３０９６４６２

Patent ☒ Trademark ☐ Docket No. 108397-00063

Serial No. New U.S. Pat Appln Filed January 29, 2002

Applicant(s) Yoshihiro Takemae

Papers filed herewith on January 29, 2002

- ☒ Fees $ 780.00
- ☒ New Application 40 pages
- ☐ Amendment
- ☐ Notice of Appeal
- ☒ IDS/PTO-1449 1 ref
- ☐ Other

- ☒ Assignment
- ☒ Declaration
- ☒ Priority Document 1
- ☐ Req. for Ext. of Time
- ☒ Drawings 17 17 sheets

Receipt is hereby acknowledged of the papers filed as indicated in connection with the above-identified case.

Cmmiars

COMMISSIONER OF PATENTS

PK

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	Confirmation No.: 2535
Yoshihiro TAKEMAE	Group Art Unit: 2185
Application No.: 10/687,591	Examiner: Daniel Y. KIM
Filed: October 20, 2003	Attorney Docket No.: 108397-00109
For: MEMORY SYSTEM	

REQUEST FOR ACKNOWLEDGEMENT OF INFORMATION DISCLOSURE STATEMENT

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 13, 2006

Sir:

In the Notice of Allowability dated October 26, 2006, the Examiner indicated that the updated copy of the Information Disclosure Statement with Form PTO-1449 filed on October 20, 2003, has not been considered because the Examiner alleges that a copy of the reference was not submitted in this application or in any related application. However, Applicant respectfully submits that the reference was cited in the Office Action dated February 4, 2003, in parent Application Number 10/057,989, now U.S. Patent Number 6,650,593 B2.

Accordingly, the Examiner is respectfully requested to initial and return to the undersigned a copy of the subject Form PTO-1449. For the convenience of the Examiner, copies of the Information Disclosure Statement, Form PTO-1449 and reference are attached.

Should there be any questions concerning this communication, please telephone the undersigned attorney at the telephone number set forth below.

Please charge any fee deficiency or credit any overpayment with respect to this paper to Deposit Account Number 01-2300, referencing Attorney Docket Number 108397-00109.

Respectfully submitted,

Charles M. Marmelstein
Registration Number 25,895

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Telephone: 202-857-6000
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CMM/SCO:vmh

Enclosures: Information Disclosure Statement
Form PTO-1449
Reference (1)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Yoshihiro TAKEMAE

Serial No.: New Application

Filed: October 20, 2003

For: MEMORY SYSTEM

Confirmation No.:

Group Art Unit:

Examiner:

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

October 20, 2003

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the information item(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each item(s) is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the item(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date or the date of filing a CPA, OR (b) before the mailing date of a first Office Action on the merits in the present application, or (c) accompanies a Request for Continued Examination. No certification or fee is required.

☐ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

☐ a. I hereby certify that each item of information contained in this Information Disclosure Statement was cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☐ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

☐ c. A check in the amount of $180.00 in payment of the fee under 37 CFR §1.17(p). Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300 as needed to ensure consideration of the disclosed information.

☐ 3. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Applicant(s) hereby petition(s) that the Information Disclosure Statement be considered. Attached is our check in the amount of $130.00 in payment of the petition fee under 37 CFR §1.17(i)(1). Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300 as needed to ensure consideration of the disclosed information.

☐ a. I hereby certify that each item of information contained in this Information Disclosure Statement was cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

☐ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

☒ 4. The references were cited by or submitted to the Office in parent application No. 10/057,989, filed January 29, 2002, which is relied upon for an earlier filing date under 35 U.S.C. §120. Thus, copies of these references are not attached. 37 CFR §1.98(d).

Respectfully submitted,

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC

Raymond J. Ho
Registration No. 41,838

Atty. Docket No.: 108397-00109

1050 Connecticut Avenue, N.W., Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

RH:mmg

Enclosure: PTO-1449 Form

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
108397-00109	New Appln.
APPLICANT: Yoshihiro TAKEMAE	
FILING DATE: October 20, 2003	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA	6,480,947 B1	11/12/02	HASEGAWA et al			
	AB						
	AC						
	AD						
	AE						
	AF						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	NO	PART.
	AG	6-42263	6/01/94	Japan					XX
	AH								
	AI								
	AJ								
	AK								
	AL								

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AM	Betty Prince, "Semiconductor Memories", 1983, Wiley, 2nd edition, pgs. 64 - 66.
	AN	
	AO	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

conventional techniques. The technique used is a repeated character learning method called back-propagation learning algorithm where the neural network checks characters and corrects them if necessary before the character is output by the system. Such a system would be expected to use RAM to store the characters during comparison.

3.7 EXAMPLE OF TYPICAL COMPUTER MEMORY STORAGE CONFIGURATION

Many of the various ways of using memory in a system can be illustrated by the Sony NEWS network station which is shown in Figure 3.10. This workstation uses two 32 bit microprocessors, a CPU and an I/O processor in a master–master arrangement. It has a version of Unix, integrates into an Ethernet local area network, is multiprocessor, has a multiwindow user environment, and supports graphics. It has a SCSI bus between the peripherals and the main memory, a VME interface bus for VME peripherals, and NFS to provide distributed processing among networked stations.

Memory devices or functions in this system include the following:

(a) An 8k byte instruction cache using a 35 ns 8k × 8 static RAM which allows the I/O processor to operate at 16.67 MHz (60 ns average cycle time) with no wait states. This is achieved by averaging the time for instructions obtained from the fast SRAM cache at 35 ns access and from the slower dynamic RAM in the main memory at 120 ns (one wait state). Even with a relatively low hit rate in the cache, the 60 ns average cycle time is achievable. Clearly the 16 bit and 32 bit system buses require the wide × 8 memory.

(b) The I/O processor provides memory management for its program memory which is a 128k × 8 SRAM on the 32 bit processor bus. This can be a slower than 100 ns memory since it is used in communicating mainly with slower peripheral devices. The isolation of the I/O processor and its program memory from the main memory bus means that operation of the CPU is slowed down only during data transfer and communication between the two processors.

(c) The 32 bit I/O processor and its program memory are isolated from the 16 bit I/O bus by a 16k byte bidirectional transmission and reception buffer which has a capacity of 10 data packets. This buffer could be implemented with a serial memory.

(d) The main memory is shared by the two processors. Part of the 8Mb of main memory is reserved for communications between the two processors. Commands from either processor pass through this section of the memory. Either processor

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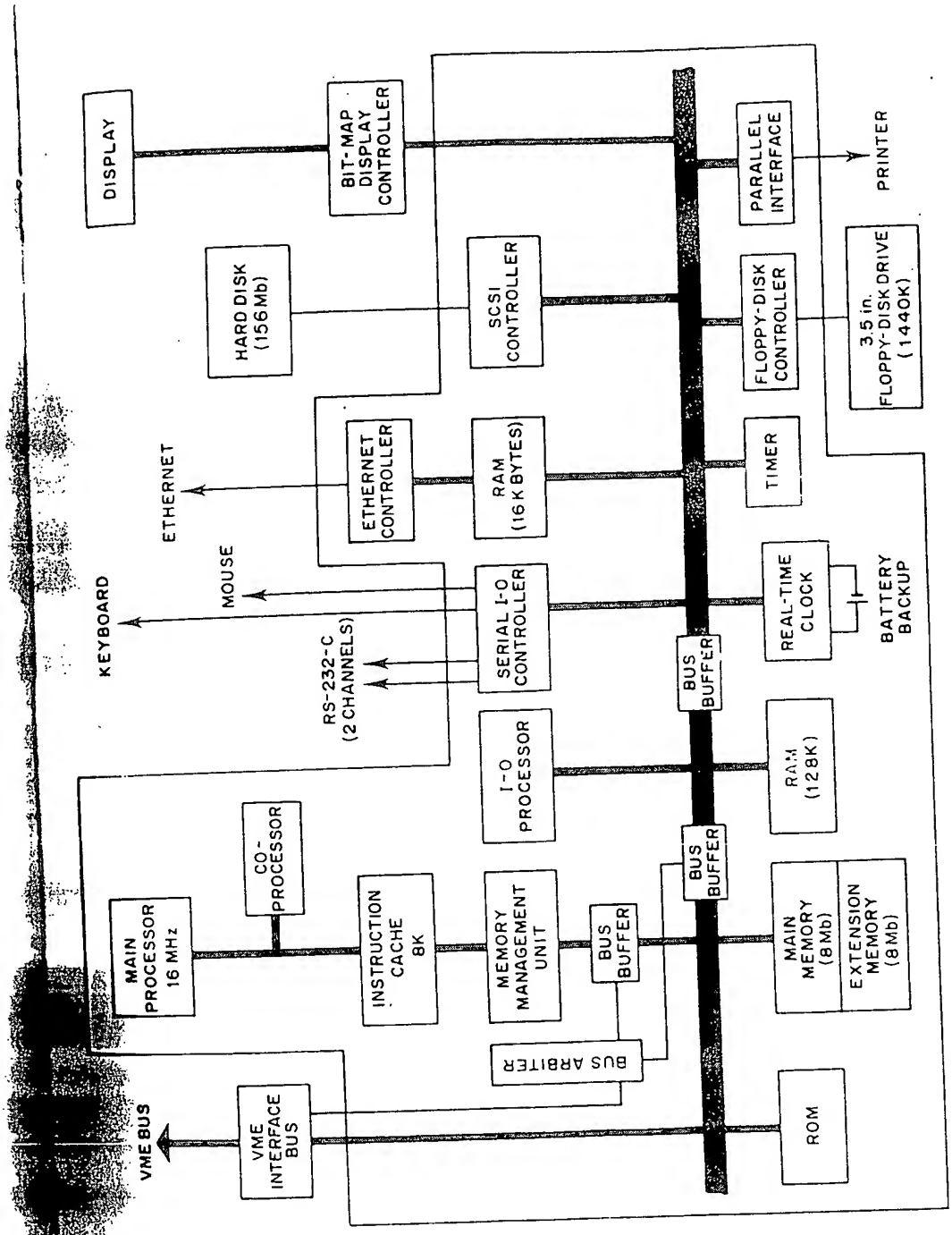

Figure 3.10
Typical bus oriented system configuration highlighting memory usage. (From Electronics [6] 1987, Sony Corporation.)

can transmit an interrupt signal. Interrupt signals are used when two processors can access the same memory location at the same time to avoid an indeterminate state occurring in that memory location if one tries to read while the other is writing. Another feature which can be used in a memory system, where contention between two processors accessing the same bit of memory is possible, is a 'busy' signal which indicates that the data location is being accessed.

(e) The memory management unit gives the system single level paging, virtual memory architecture. It supports demand-paging virtual memory. The MMU acts as a 35 ns cache for faster access of the pages in most recent use. One level paging with a page size of 4k bytes is used. The originals of the MMU page-table entries are stored in the main memory and the MMU serves as the cache for faster access of these pages.

(f) The high speed multiwindow display system requires hardware with the 'bit boundary block' (bitblt) transfer function for the bit-map displays. This could be implemented either in an applications specific memory, or, as in this case, with a 2000 gate array. The color display uses one gate array to hold the current data for each color plane all of which operate concurrently so that multiwindow processing in color can be done as fast as for monochrome.

(g) There is an option for connecting peripherals on a VME bus. In a master–slave arrangement, the CPU operates as master for controlling access to the peripherals. Both addresses and data words are 32 bits wide.

(h) Archive files are provided with 156Mb of hard disk and a 1440k byte floppy disk drive, both on the 8 bit SCSI control bus. This bus is capable of parallel data transfer at 1.5 Mb s^{-1} (or 83 ns/bit data rate) for asynchronous transmission and 4 Mb s^{-1} for synchronous. This very slow data rate and large size of memory means that a high density, low cost alternative must be chosen for the archive memory. Clearly either optical or magnetic memory could be used for the hard disk.

(i) The system also supports distributed processing, or networking. The directories of the memory files from a remote machine can be entered in the users machine and accessed just like local files through a virtual file system in the Unix.

(j) The system also supports Ethernet using 16k bytes of SRAM in this interface onto the 16 bit peripherals bus.

(k) Finally, the system contains a real-time clock which can store the time either in static RAM with battery back-up or in an EEPROM. In this particular system SRAM with battery back-up was used.